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PATENT

4-23-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		
Jeffrey S. Mailloux et al.		Examiner: Hong C. Kim
Serial No.:	08/984,560	Group Art Unit: 2186
Filed:	December 3, 1997	Docket: 303.623US2
For:	MEMORY DEVICE WITH PATTERNED AND PATTERNLESS ADDRESSING	

APPELLANTS' BRIEF ON APPEAL

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on February 14, 2003, from the Final Rejection of claims 11-21 and 59-71 of the above-identified Application, as set forth in the Final Office Action mailed January 22, 2003.

This Appeal Brief is filed in triplicate and accompanied by the requisite fee set forth in 37 C.F.R. § 117(c). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims 11-21 and 59-71.

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are three other appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. These related appeals are currently pending before the Board and concern U.S. Patent Application Serial Numbers 08/984,561; 08/984,562; and 08/984,701.

3. STATUS OF THE CLAIMS

Claims 11-21 and 59-71 are currently pending. Claims 11-21 and 59-71 stand rejected and are appealed.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action mailed to the Appellants on January 22, 2003. However, the Board is asked to consider the following amendments which provide clarity and consistency, and are not related to patentability:

59. (Amended) A memory device, comprising:
a memory array;
control logic operatively connected to the memory array, the control logic for selecting between an unpatterned pipeline scheme and a patterned burst scheme [data pattern] for accessing the memory array; and
switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected.

61. (Amended) A dynamic random access memory, comprising:
a plurality of addressable memory arrays;
a column address decoder for receiving an external column address;
control logic operatively coupled to the plurality of addressable memory arrays and the column address decoder for selecting between a burst or a pipeline mode of operation [based];
switching circuitry for switching between a burst pathway and a pipeline pathway depending on which of the burst or pipeline modes of operation is selected.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates in either burst or pipelined modes. In one embodiment, an asynchronously addressable storage device 100 (Application, FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Application, Pg. 29, lines 5-25).

Some embodiments of the invention can switch between burst access and pipelined modes of operation without ceasing ("on the fly"). (Application, Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is used to select data within the device 100. A counter 149 included in the circuitry 122 increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses only external addresses 115 to access data within the device 100. (Application, Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Application, Pg. 8, lines 1-5). In addition to the embodiment described, other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits, are discussed. (Application, Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

Whether claims 11-21 and 59-71 were properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter "Manning").

Whether U.S. Patent No. 5,610,864, issued to Manning on March 11, 1997, is properly characterized as prior art under 35 U.S.C. § 102(b) or 35 U.S.C. § 102(e) since the priority filing date of the present patent application is May 20, 1996.

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal. For a complete statement of support for this grouping, see section c.2 below.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

b) The Reference

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address.

(Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of the structure of the architecture, how it is applied, or its operation, are given.

U.S. Patent No. 5,610,864, issued to Manning on March 11, 1997. The priority filing date of the present patent application is May 20, 1996. The Manning reference is assigned to the same assignee as the present patent application. At the time of the invention of the Manning patent, the inventors of that patent were under a duty to assign their inventions to the same assignee as the present patent application. At the time of the present inventions, the inventors were under a duty to assign their inventions to the same assignee as in the Manning patent.

c) Discussion of the Rejections

***c.1* -- The rejection under § 102**

Claims 11-21 and 59-71 were rejected under 35 U.S.C. § 102(b) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art under 35 U.S.C. § 102(b) and reserve the right to swear behind this reference in the future since the Manning reference should be characterized under 35 U.S.C. § 102(e). Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(b) has not been made because Manning does not disclose each and every element of claims 11-21 and 59-71. Therefore, the Appellants respectfully traverse this rejection under 35 U.S.C. § 102(b).

c.1.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning does not disclose "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected," as recited in independent claims 11, 62, 65 and 68 (and dependent claims 12-21, 63-64, 66-67, and 69). While Fig. 1, Ref. 38; Col. 5, lines 43-50; Col.

6, lines 14-32; and Col. 7 lines 43-54 of Manning have been cited in the Office Action to support the disclosure of the claimed switching circuitry, the Appellants' representative is unable to find this kind of circuitry anywhere within the bounds of the reference.

Fig. 1, Ref. 38 is a block labeled generic DRAM control logic, with no indication whatsoever regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 43-50 discuss the possibility of using a pipelined architecture, but not as enabling switching between patterned and patternless, or pipeline and burst operations, on-the-fly, within the same memory, as disclosed and claimed by the Appellants (e.g., perhaps Manning refers to a pipelined *output* stage of a burst EDO device? see below ...). Col. 6, lines 14-32 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode.

Similarly, it has been asserted in the Office Action that Manning discloses "switching circuitry for switching between a first ... pathway and a second ... pathway depending on which of said pipeline scheme and said burst scheme is selected" as claimed in independent claim 59, or "switching circuitry for switching between a ... burst ... pathway and a ... pipeline ... pathway" as claimed in independent claims 60, 61, and 70 (and independent claim 71). Again, the Appellants' representative was unable to find any portion of Manning to support the idea that Manning includes such circuitry. Thus, no *prima facie* case of anticipation has been established.

Several other assertions were made which attribute support to various concepts allegedly disclosed by Manning in the Office Action. However, a careful reading of each citation reveals that the discussion of the asserted elements is in error. These assertions have been made with respect to:

Claims 13 - Manning does not disclose a temporary buffer for providing an external address as element 34 (this element in Manning is a latch for data and chip control signals).

Claim 19 - Manning does not disclose switching circuitry having a multiplexed device (FIG. 5 of Manning referenced in the Office Action describes a write timing circuit, not mode switching circuitry).

Claim 20 - Manning does not disclose random CAS signals as part of the pipelined architecture (Manning merely refers to the possibility of using a pipelined architecture, not how it operates, see below).

Claims 59, 60 - Manning does not disclose control logic for selecting between burst and pipelined modes of operation (since Manning does not disclose a pipelined mode of operation).

Claims 11, 59-62, 65, 68, 70 - Manning does not disclose switching between two pathways in conjunction with patterned and patternless, or burst and pipelined modes (the Office has not asserted the existence of such pathways, and Manning does not disclose them).

Claim 64 - Manning does not disclose a pipeline extended data out pattern (Manning only teaches the possibility of a pipelined architecture, see below).

Finally, four erroneous assertions have been directed toward all pending claims. First, it is not true that one must "select pipeline mode" to "work in the pipeline architecture" (See Paper 28, page 8 - the assertion is erroneous because the pipelined mode does not need to be selected if a device always operates in that mode). Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward "a storage device", "a memory device", or a "a dynamic random access memory". Third, while the assertion is made that "one of ordinary skill in the art at the time the invention was made would have been lead to an obvious fashion to provide a pipelined page mode circuitry", it is respectfully noted that this reasoning does not comport with the standard set by § 102 - it is only appropriate for a rejection based upon § 103. Fourth, the introduction of a second reference to provide support for an element not present in Manning (U.S. Patent No. 5,966,724) also does not comport with the standard set by § 102. Again, this type of argument is only appropriate for a rejection based upon § 103.

c.1.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

As noted above, it is asserted in the Office Action that "... in order to work in the pipeline architecture one has to select pipeline mode." This is not true, since a memory including a pipeline architecture may operate according to that architecture (which is not necessarily the

same thing as the pipelined mode) without any switching or selection whatsoever, especially if that is the fixed mode of operation for that memory. Thus, Manning never discusses the ability to *switch or select* between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Appellants.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned in Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as part of Appendix II. The content of this article is summarized in the next few paragraphs.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new

column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory further improved EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

In embodiments of the Appellants' invention, a newburst signal from control logic is described. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with an initial external address stored in a temporal storage device. Consequently, if burst operation is the selected mode of operation, then a counter is used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through a memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

Further, the instant Application describes how to switch between data pathways, depending on whether a patternless or patterned addressing scheme is selected. Independent claims 11, 59-62, 65, 68, and 70 recite this limitation. However, this type of operation is not taught or suggested by Manning.

Finally, it is unreasonable to interpret the possible existence of a pipelined architecture in Manning's device as equivalent to operating in the pipelined mode taught and claimed by the Appellants. It is also inconsistent to admit, on the one hand, that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation" in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7), and then on the other, to state that Manning teaches control logic and/or switching circuitry to switch between pipelined and burst modes of operation in the instant Office Action. The MPEP requires that "[d]uring patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.'" See M.P.E.P. § 2111. The Appellants respectfully submit that the interpretation of the pending claims by the Office is neither reasonable nor consistent with the text of the instant specification.

Thus, what Manning discloses is not identical to the subject matter of the Appellants' invention, and the Office has failed to produce a *prima facie* case of anticipation. Therefore, the rejection under 35 USC § 102 is improper, and it is respectfully requested that the rejection of claims 11-21 and 59-71 be reconsidered and withdrawn.

c.2 -- Why the claims are separately patentable

While the separate patentability of each claim has been discussed in the "Argument" section above, as permitted by M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 11 is directed toward a storage device having "control logic for switching between a patternless addressing scheme and a patterned addressing scheme" and "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected." Manning does not disclose this combination of elements, and independent claims 59-61 do not have this unique combination of elements.

To the elements of independent claim 11, dependent claim 12 adds "the storage device is asynchronous." Manning does not disclose this combination of elements, and no other claim (except claims 13-19) has this unique combination of elements.

To the elements of dependent claim 12, dependent claim 13 adds "wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry." Manning does not disclose this combination of elements, and no other claim (except claims 14-19) has this unique combination of elements.

To the elements of dependent claim 13, dependent claim 14 adds "wherein the external address is temporarily stored in the temporary storage device prior to being sent to a decoder." Manning does not disclose this combination of elements, and no other claim (except claims 15-19) has this unique combination of elements.

To the elements of dependent claim 14, dependent claim 15 adds "further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address." Manning does not disclose this combination of elements, and no other claim (except claims 16-19) has this unique combination of elements.

To the elements of dependent claim 15, dependent claim 16 adds "wherein the internal address is provided to the temporary storage device through the switching circuitry." Manning does not disclose this combination of elements, and no other claim (except claims 17-19) has this unique combination of elements.

To the elements of dependent claim 16, dependent claim 17 adds "wherein the patternless addressing scheme provides a pipelined extended data out pattern." Manning does not disclose this combination of elements, and no other claim (except claims 18-19) has this unique combination of elements.

To the elements of dependent claim 17, dependent claim 18 adds "wherein the patterned addressing scheme provides a burst extended data out pattern." Manning does not disclose this combination of elements, and no other claim (except claim 19) has this unique combination of elements.

To the elements of dependent claim 18, dependent claim 19 adds "wherein the switching circuitry includes at least one multiplexed device." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 11, dependent claim 20 adds "wherein the patternless addressing scheme is for a random column address access, and the patterned addressing scheme is for a sequential column address access." Manning does not disclose this combination of elements, and no other claim (except claim 21) has this unique combination of elements.

To the elements of dependent claim 20, dependent claim 21 adds "wherein the sequence column address access is selected from a group consisting of an interleaved column address access and a linear column address access." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 59 (as amended) is directed toward a memory device having "a memory array", "control logic for selecting between an unpatterned pipeline scheme and a patterned burst scheme", and "switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline... and said burst scheme is selected." Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

Independent claim 60 is directed toward a memory device having "a memory array operable in a burst or a pipeline mode of operation", "control logic for selecting between the burst or the pipeline mode" and "switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway ..." Manning does not disclose this combination of elements, and no other independent claim (except for claim 70) has this unique combination of elements.

Independent claim 61 (as amended) is directed toward a dynamic random access memory having "a plurality of addressable memory arrays" and "control logic ... for selecting between a burst or a pipeline mode of operation". Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

Independent claim 62 is directed toward a storage device having "control logic for selecting between a patternless addressing scheme and a patterned addressing scheme", "a counter", and "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected." Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

To the elements of independent claim 62, dependent claim 63 adds "wherein the internal address is provided to the temporary storage device through the switching circuitry." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 62, dependent claim 64 adds "wherein the patternless addressing scheme provides a pipelined extended data out pattern." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 65 is directed toward a storage device having "control logic for selecting between a patternless addressing scheme and a patterned addressing scheme" and "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected, wherein the patternless addressing scheme provides a pipelined extended data out pattern." Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

To the elements of independent claim 65, dependent claim 66 adds "wherein the patterned addressing scheme provides a burst extended data out pattern." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 65, dependent claim 67 adds " wherein the switching circuitry includes at least one multiplexed device." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 68 is directed toward a storage device having "control logic for selecting between a patternless addressing scheme and a patterned addressing scheme" and "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected, wherein the patterned addressing scheme provides a burst extended data out pattern." Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

To the elements of independent claim 68, dependent claim 69 adds "wherein the switching circuitry includes at least one multiplexed device." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 70 is directed toward a memory having "a memory array operable in a burst mode ... or a pipelined mode", "control logic for selecting between the burst mode ... or the pipelined mode", and "switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipelined modes is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device ..." Manning does not disclose this combination of elements, and no other independent claim has this unique combination of elements.

To the elements of independent claim 70, dependent claim 71 adds "further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

9. SUMMARY

It is respectfully submitted that a case of anticipation under 35 U.S.C. §102 has not been established. Therefore, reconsideration and withdrawal of the rejections of claims 11-21 and 59-71 is respectfully requested.

The Appellants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellants' attorney, **Mark Muller at (210) 308-5677**, or the undersigned attorney, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date April 14, 2003 By Daniel J. Kluth
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Reg. No. 32,146

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner of Patents, Washington, D.C. 20231, on this 14 day of April, 2003.

Tina Kohout
Name

Signature

APPENDIX I

The Claims on Appeal

11. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected.

12. A storage device, as in Claim 11, wherein the storage device is asynchronous.

13. A storage device, as in Claim 11, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

14. A storage device, as in Claim 13, wherein the external address is temporarily stored in the temporary storage device prior to being sent to a decoder.

15. A storage device, as in Claim 14, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

16. A storage device, as in Claim 15, wherein the internal address is provided to the temporary storage device through the switching circuitry.

17. A storage device, as in Claim 16, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

18. A storage device, as in Claim 17, wherein the patterned addressing scheme provides a burst extended data out pattern.

19. A storage device, as in Claim 18, wherein the switching circuitry includes at least one multiplexed device.

20. A storage device, as in Claim 11, wherein the patternless addressing scheme is for a random column address access, and the patterned addressing scheme is for a sequential column address access.

21. A storage device, as in Claim 20, wherein the sequence column address access is selected from a group consisting of an interleaved column address access and a linear column address access.

59. A memory device, comprising:

a memory array;

control logic operatively connected to the memory array, the control logic for selecting between an unpatterned pipeline and a patterned burst data pattern for accessing the memory array; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected.

60. A memory device, comprising:

a memory array operable in a burst or a pipeline mode of operation;

control logic for selecting between the burst or the pipeline mode of operation; and

switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipeline modes of operation is selected.

61. A dynamic random access memory, comprising:

a plurality of addressable memory arrays;

a column address decoder for receiving an external column address;

control logic for selecting between a burst or a pipeline mode of operation based;

switching circuitry for switching between a burst pathway and a pipeline pathway depending on which of the burst or pipeline modes of operation is selected.

62. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme;

a counter; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry, and wherein the counter is coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

63. The storage device of Claim 62, wherein the internal address is provided to the temporary storage device through the switching circuitry

64. The storage device of Claim 62, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

65. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme

is selected, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

66. The storage device of Claim 65, wherein the patterned addressing scheme provides a burst extended data out pattern.

67. The storage device of Claim 65, wherein the switching circuitry includes at least one multiplexed device.

68. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the patterned addressing scheme provides a burst extended data out pattern.

69. The storage device of Claim 68, wherein the switching circuitry includes at least one multiplexed device.

70. A memory device, comprising:

a memory array operable in a burst mode of operation or a pipelined mode of operation;

control logic for selecting between the burst mode of operation or the pipelined mode of operation; and

switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipelined modes of operation is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

71. The memory device of Claim 70, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

APPENDIX II

Other References

"Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999

Company

Shuttle Connecting Technology

Home Company News Products Support Awards Certificates Comments Employment Where to buy

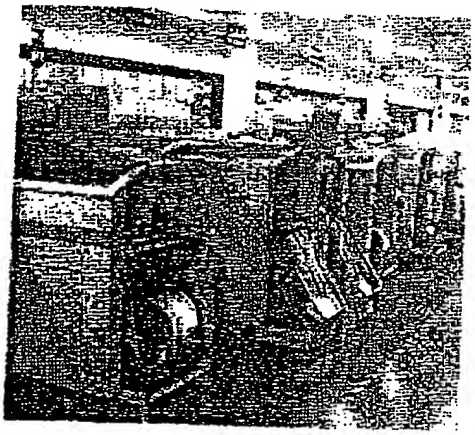
SHUTTLE - Your Ultimate Source for PC

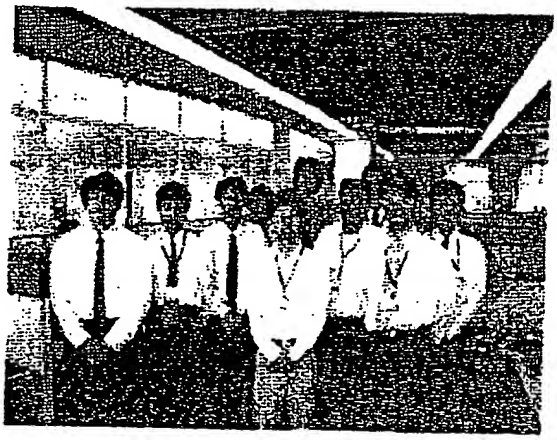
SHUTTLE INC., headquarters of Shuttle Gro Taiwan based manufacturer and supplie mainboards and add-in cards. Ever since its 1983, SHUTTLE has always been recc international markets for delivering produc technology together with exceptional quality a Today, SHUTTLE has become one of the manufacturers in the world with sales rever US$200 millions. Its Shuttle ™ and Spacewa have already reached millions of satisfied c widel

Sales, Service and Support

SHUTTLE is a multi-national company with a strong commitment in customer service. Regional sales offices are located in the United States, Germany, Italy, Poland and Taiwan. Localization plus reliable after sales service and prompt technical support have enabled SHUTTLE to maintain a strong relationship with its customers including system integrators, VARs, OEMs, ODMs and distribution network.

In order to ensure round-the-clock service & support, SHUTTLE is accessible by E-mail, Web site and BBS.





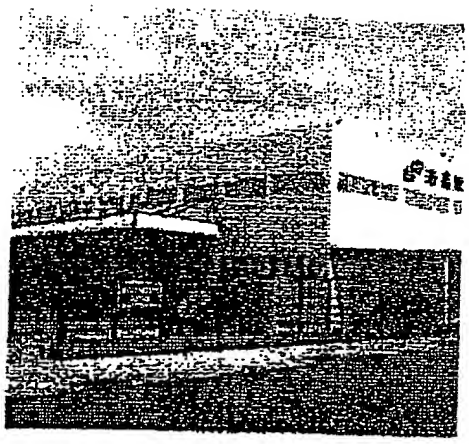
Research and Development

The Research and Development engineers highly experienced and creative. For 1! professionals are always in pursuit of i maintaining product's price per performance quality. Fully equipped with hi-end CAD too intensive research of up-to-date technology, professionals at SHUTTLE have provided super have been proven in the market for over a dec

Manufacturing

SHUTTLE is dedicated to TQM (Total Quality Management) principles. Only genuine brand name components are used in the products and strict QA/QC procedures are followed in the

manufacturing process. The manufacturing facilities feature the latest in SMT equipment and manufacturing technology. ISO9001, ISO9002, and ISO14000 certified, SHUTTLE's factories yield the total production capacity of over 300K units per month. In order to keeping pace with its rapidly expanding global markets, SHUTTLE is in the process of increasing its manufacturing capacity as additional SMT lines are implemented.



Environmental Policy

Our company is a member of the global together with the whole global enterprises t the green environment. We are dedicated protection of the environment and the environmental pollution, for the minimizing o handling of energy conservation, as well as to related legal requirements. This is to allow th be able to have our manufactured green p eventually protect our environment.

Our commitments:

- Strictly implement the laws and regulations
- Continuously improve the measures for preventing pollution
- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products

Commitment to Customers

SHUTTLE strongly believes in teamwork partnership with customers and remains firmly committed to delivering products with the highest quality, optimum performance and value.

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FAX: 626-820-5060
http://www.shuttleonline.com

Germany Sales Office:
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FAX: 49-4121-476900

Frequently Asked Questions

SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

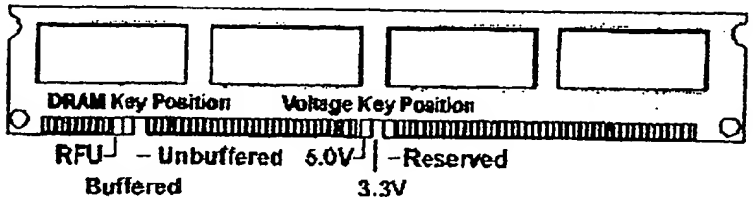
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

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